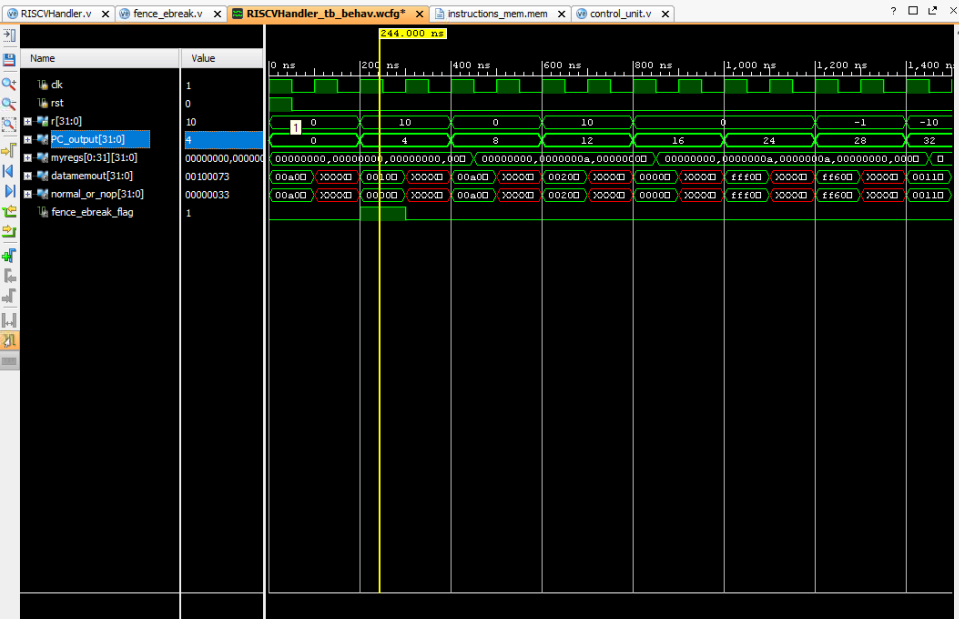
Ebreak and Fence

**EBREAK**

Note that at clock cycle three, the ebreak is fetched and we can observe from the simulation that the single memory is spitting out the hexadecimal value of the ebreak instruction and the fence\_ebreak\_flag is set so the output of the mux after the single memory outputs a nop instruction that will be fed into the IF\_ID register in the pipeline.

This is the hexadecimal value for the EBREAK:

0x00100073



The testing code:

93 00 A0 00

73 00 10 00

13 01 A0 00

The equivalent assembly code:

Addi x1, x0, 10

Ebreak

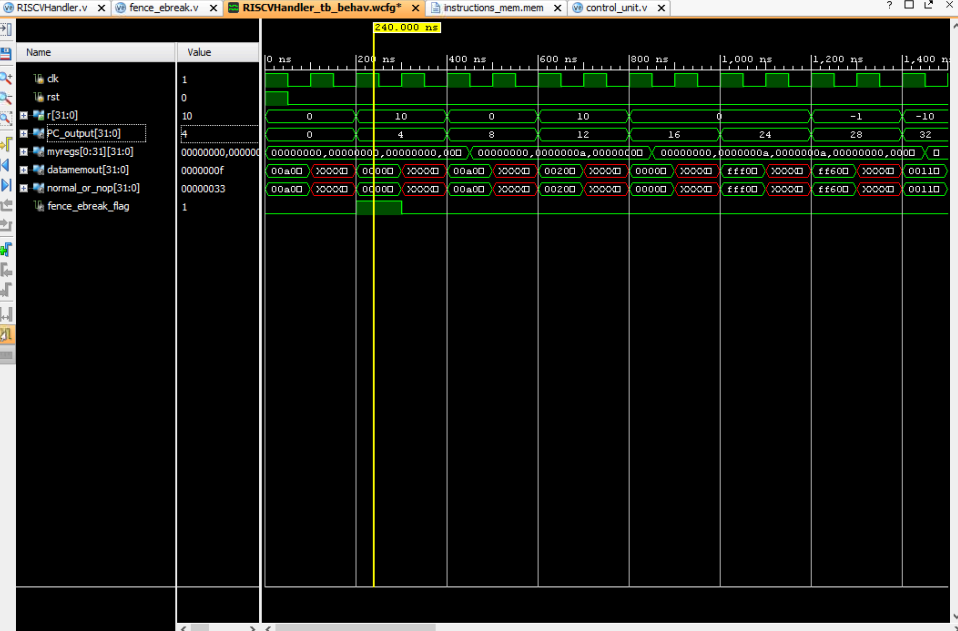
Addi x2, x0, 10

**FENCE:**

Note that at clock cycle three, the fence instruction is fetched and we can observe from the simulation that the single memory is spitting out the hexadecimal value of the fence instruction while the fence\_ebreak\_flag is set so the output of the mux after the single memory outputs a nop instruction that will be fed into the IF\_ID register in the pipeline.

This is the hexadecimal value for the FENCE:

0x0000000F



The testing code:

93 00 A0 00

0f 00 00 00

13 01 A0 00

The equivalent assembly code:

Addi x1, x0, 10

Fence 1,1

Addi x2, x0, 10